

SANYO	No.3030A	LB8901M
	CCD Clock Driver	

Overview

- The LB8901M is a monolithic IC designed to drive large-capacity clock gates of a CCD image sensor (LC9900 series) at a high speed.

Features

- Capable of driving large-capacity gates of a CCD, etc.
- On-chip eight-block driver, two of which are capable of providing drive on the three-value level (LC9900 series). No more than one chip is required to drive vertical gates.
- Placed in a 24-pin miniflat package (MFP24S), facilitating miniaturization of equipment.
- Capable of being driven direct with TTL, CMOS, etc.
- A power save circuit can be connected to permit less power dissipation.

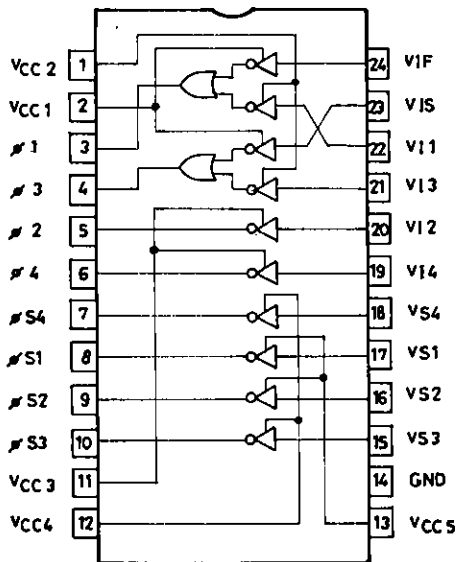
Absolute Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V _{CC} max	Each V _{CC} pin	-0.3 to +18.0	V
Input Supply Voltage	V _{IN}	Each input pin	-0.3 to +6.0	V
Maximum Output Current	I _{OUT}	Each output pin	250	mA
Allowable Power Dissipation	Pd max		620	mW
Operating Temperature	T _{opr}		-10 to +70	°C
Storage Temperature	T _{stg}		-40 to +125	°C

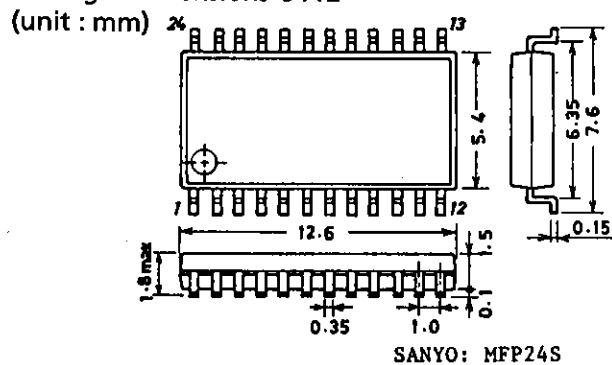
Allowable Operating Conditions at Ta = 25°C

				unit
Supply Voltage	V _{CC}	Each V _{CC} pin	5 to 18	V
	ΔV _{CC1-2}	V _{CC1} - V _{CC2} voltage difference	0 to 6.0	V
Input 'H'-Level Voltage	V _{IH}	Each input pin	2.5 to 6.0	V
Input 'L'-Level Voltage	V _{IL}	Each input pin	-0.3 to +0.3	V

Equivalent Circuit Block Diagram



Package Dimensions 3112



LB8901M

Electrical Characteristics at Ta = 25°C, VCC1 = 9.0V, VCC2 to 5 = 13.0V			min	typ	max	unit
Input 'H'-Level Current	I _{IH1}	V _{I1} , V _{I3} inputs of blocks 1,2 V _{IN} = 5.0V		1.0	2	mA
	I _{IH2}	V _{IF} , V _{IS} inputs of blocks 1,2 V _{IN} = 5.0V		1.0	2	mA
	I _{IH3}	V _{I2} , V _{I4} inputs of blocks 3,4 V _{IN} = 5.0V		1.0	2	mA
	I _{IH4}	V _{S1} to 4 inputs of blocks 5 to 8 V _{IN} = 5.0V		1.0	2	mA
Input 'L'-Level Current	I _{IL1}	V _{I1} to 4, V _{S1} to 4 inputs of blocks 1 to 8 V _{IN} = 0V	-30			μA
	I _{IL2}	V _{IF} , V _{IS} inputs of blocks 1,2 V _{IN} = 0V	-100	-20		μA
Supply Current	I _{CCH1}	Each input ; V _{IN} = 5.0V		0.5	1	mA
	I _{CCH2}	Each input ; V _{IN} = 5.0V		4.0	8	mA
	I _{CCH3}	Each input ; V _{IN} = 5.0V		4.0	8	mA
	I _{CCH4}	Each input ; V _{IN} = 5.0V		4.0	8	mA
	I _{CCH5}	Each input ; V _{IN} = 5.0V		4.0	8	mA
	I _{CCCL1}	Each input ; V _{IN} = 0V			300	μA
	I _{CCCL2}	Each input ; V _{IN} = 0V			100	μA
	I _{CCCL3}	Each input ; V _{IN} = 0V			100	μA
	I _{CCCL4}	Each input ; V _{IN} = 0V			100	μA
	I _{CCCL5}	Each input ; V _{IN} = 0V			100	μA
Output Voltage	V _{OH1}	V _{I1} = 0V, V _{IF} = 5V	V _{CC2} - 2.0			V
	V _{OH2}	V _{I1} = 0V, V _{IF} = 0V	V _{CC1} - 1.0			V
	V _{OH3}	V _{I3} = 0V, V _{IS} = 5V	V _{CC2} - 2.0			V
	V _{OH4}	V _{I3} = 5V, V _{IS} = 0V	V _{CC1} - 1.0			V
	V _{OH5}	V _{I2} , V _{I4} = 0V	V _{CC3} - 2.0			V
	V _{OH6}	V _{S3} , V _{S4} = 0V	V _{CC4} - 2.0			V
	V _{OH7}	V _{S1} , V _{S2} = 0V	V _{CC5} - 2.0			V
	V _{OL}	Each input V _{IN} = 5V			1.0	V

Switching Characteristics at Ta = 25°C, VCC1 = 9.0V, VCC2 to 5 = 13.0V, V_{IN} = 5.0V, t_r, t_f ≤ 10ns

			min	typ	max	unit
Propagation Time 'L'-Level → 'H'-Level	t _{PLH1}	Ø1,3 outputs ; V _{IF} , V _{IS} = 5.0V fixed		30		ns
	t _{PLH2}	Ø1,3 outputs ; V _{I1} , V _{I3} = 5.0V fixed		2		μs
	t _{PLH3}	Ø2,4, ØS1 to 4 outputs		30		ns
Propagation Time 'H'-Level → 'L'-Level	t _{PHL1}	Ø1,3 outputs ; V _{IF} , V _{IS} = 5.0V fixed		30		ns
	t _{PHL2}	Ø1,3 outputs ; V _{I1} , V _{I3} = 5.0V fixed		1		μs
	t _{PHL3}	Ø2,4, ØS1 to 4 outputs		30		ns
Transient Rise Time	t _{r1}	Ø1,3 outputs ; V _{IF} , V _{IS} = 5.0V fixed		30		ns
	t _{r2}	Ø1,3 outputs ; V _{I1} , V _{I3} = 5.0V fixed		6		μs
	t _{r3}	Ø2,4, ØS1 to 4 outputs		30		ns
Transient Fall Time	t _{f1}	Ø1,3 outputs ; V _{IF} , V _{IS} = 5.0V fixed		30		ns
	t _{f2}	Ø1,3 outputs ; V _{I1} , V _{I3} = 5.0V fixed		300		ns
	t _{f3}	Ø2,4, ØS1 to 4 outputs		30		ns

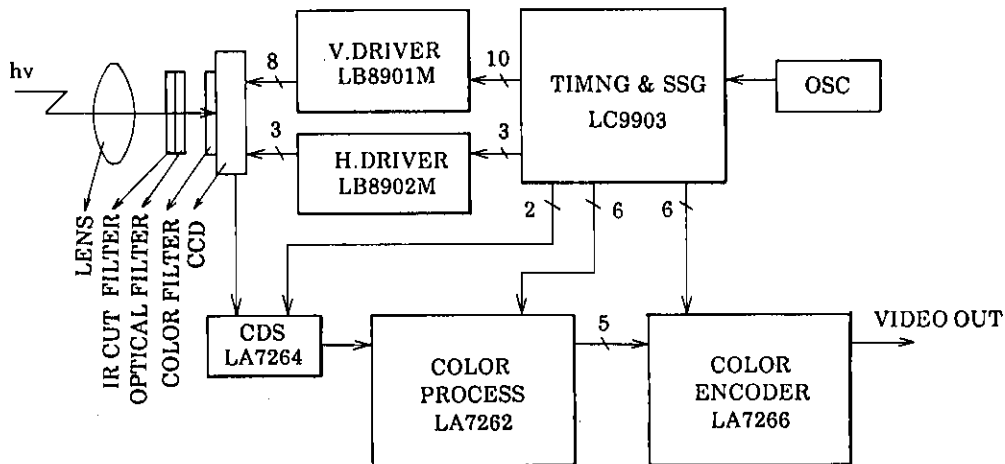
Note : Load conditions

- Positive three-value driver (Ø1,3) ----- RS = 16Ω, C_L = 1200pF
- Positive two-value driver (Ø2,4, ØS1 to 4) ----- RS = 20Ω, C_L = 1300pF

LB8901M Pin Assignment

Pin No.	Pin Name	Pin Description
1	V _{CC2}	Power supply for frame shift pulse at ϕ 1,3
2	V _{CC1}	Power supply for three-value pulse at ϕ 1,3
3	ϕ 1	Positive three-value drive output, for ϕ 1 of CCD
4	ϕ 3	Positive three-value drive output, for ϕ 3 of CCD
5	ϕ 2	Positive two-value drive output, for ϕ 2 of CCD
6	ϕ 4	Positive two-value drive output, for ϕ 4 of CCD
7	ϕ S4	Positive two-value drive output, for ϕ S4 of CCD
8	ϕ S1	Positive two-value drive output, for ϕ S1 of CCD
9	ϕ S2	Positive two-value drive output, for ϕ S2 of CCD
10	ϕ S3	Positive two-value drive output, for ϕ S3 of CCD
11	V _{CC3}	Power supply for ϕ 2,4
12	V _{CC4}	Power supply for ϕ S3,S4
13	V _{CC5}	Power supply for ϕ S1,S2
14	GND	Ground pin
15	V _{S3}	Clock input for ϕ S3 driver
16	V _{S2}	Clock input for ϕ S2 driver
17	V _{S1}	Clock input for ϕ S1 driver
18	V _{S4}	Clock input for ϕ S4 driver
19	V _{I4}	Clock input for ϕ 4 driver
20	V _{I2}	Clock input for ϕ 2 driver
21	V _{I3}	Clock input for ϕ 3 driver
22	V _{I1}	Clock input for ϕ 1 driver
23	V _{IS}	Three-value pulse input for ϕ 3 driver
24	V _{IF}	Three-value pulse input for ϕ 1 driver

Sample Application Circuit : Camera Block Diagram



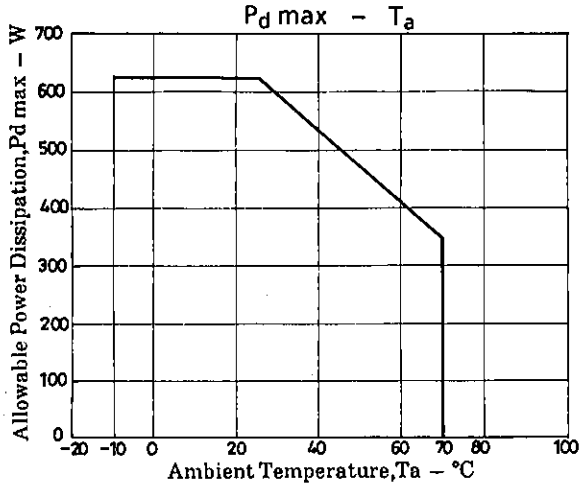
Proper Cares to be Taken in Designing a Printed Circuit Board

The LB8901M draws a large instantaneous current when it drives a load. The LB8901M is also designed to drive a load at a very high speed. When designing a printed circuit board, keep in mind the following points to prevent the output waveforms from being adversely affected.

- 1) Make the pattern of the power supply, GND lines as large as possible.
- 2) Place the bypass capacitor as close to the IC as possible (less than 1cm).
- 3) Make the wiring of the input signal line as short as possible to minimize the effect of stray capacitance.
- 4) Make the wiring of the output signal line also as short as possible, because the inductance of a long signal line may affect the output waveforms adversely.

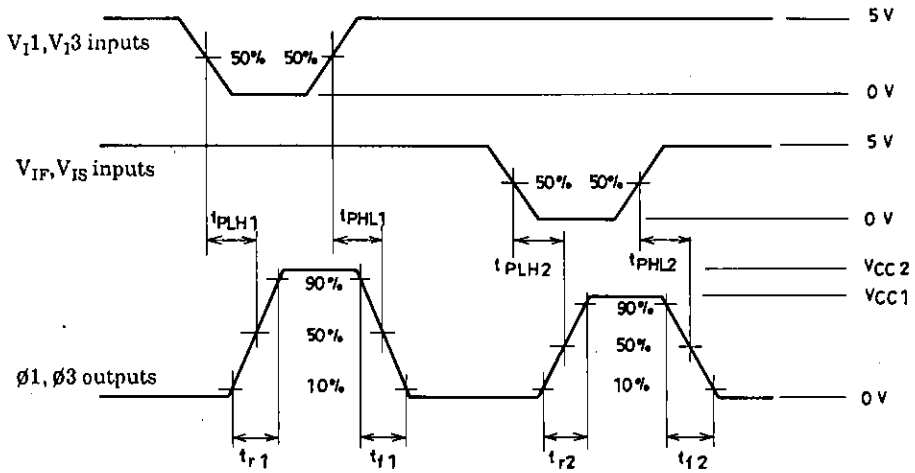
Take such necessary measures that a small resistance is inserted in series with a load.

- 5) When using a power save circuit, place it also as close to the IC as possible.



Switching Waveforms

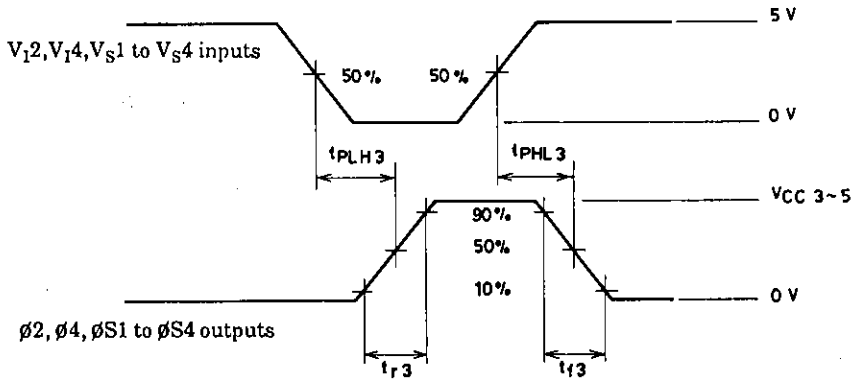
1) Blocks 1,2



Truth Table

		V _{IF} , V _{IS} inputs	
		HIGH	LOW
V _{I1} , V _{I3} Input	HIGH	V _{OL}	V _{OH2,4}
	LOW	V _{OH1,3}	Inhibit

2) Blocks 3 to 8



Truth Table

		Output
		V _{OL}
Input	HIGH	V _{OH5 to 7}
	LOW	V _{OH5 to 7}

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